

TFT LCD Tentative Specification

MODEL NO.: N141I1 - L04

Customer:

Approved by:

Note:

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
	



- CONTENTS -

REVISION HISTORY	3
1. GENERAL DESCRIPTION	4
1.1 OVERVIEW	
1.2 FEATURES	
1.3 APPLICATION	
1.4 GENERAL SPECIFICATIONS	
1.5 MECHANICAL SPECIFICATIONS	
2. ABSOLUTE MAXIMUM RATINGS	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	
2.2 ELECTRICAL ABSOLUTE RATINGS	
2.2.1 TFT LCD MODULE	
2.2.2 BACKLIGHT UNIT	
3. ELECTRICAL CHARACTERISTICS	7
3.1 TFT LCD MODULE	
3.2 BACKLIGHT UNIT	
4. BLOCK DIAGRAM	11
4.1 TFT LCD MODULE	
4.2 BACKLIGHT UNIT	
5. INPUT TERMINAL PIN ASSIGNMENT	12
5.1 TFT LCD MODULE	
5.2 BACKLIGHT UNIT	
5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL	
5.4 COLOR DATA INPUT ASSIGNMENT	
5.5 EDID DATA STRUCTURE	
6. INVERTER SPECIFICATION	16
6.1 CONNECTOR TYPE	
6.2 INPUT CONNECTOR PIN ASSIGNMENT	
6.3 OUTPUT CONNECTOR PIN ASSIGNMENT	
6.4 GENERAL ELECTRICAL SPECIFICATION	
7. INTERFACE TIMING	22
7.1 INPUT SIGNAL TIMING SPECIFICATIONS	
7.2 POWER ON/OFF SEQUENCE	
8. OPTICAL CHARACTERISTICS	24
8.1 TEST CONDITIONS	
8.2 OPTICAL SPECIFICATIONS	
9. PRECAUTIONS	28
9.1 HANDLING PRECAUTIONS	
9.2 STORAGE PRECAUTIONS	
9.3 OPERATION PRECAUTIONS	
10. PACKING	29
10.1 CARTON	
10.2 PALLET	



11. DEFINITION OF LABELS

11.1 CMO MODULE LABEL

11.2 CMO CARTON LABE

31

**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
0.0	Jun, 15,'05	All	All	Tentative specification was first issued.
0.1	Jul, 15, '05	7	2.2.2	Update lamp current
		10	3.2	Update lamp current and operating frequency
		24	8.1	Update test condition: inverter driving frequency
		24	8.2	Update optical specification: contract ratio, white variation, color chromaticity

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N141I1 - L04 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1280 x 800 WXGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA (1280 x 800 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	303.36(H) X 189.6(V)	mm	(1)
Bezel Opening Area	306.76 (H) x 192.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.237 (H) x 0.237 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti-glare , Haze 26,3H	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	319	319.5	320	mm	(1)
	Vertical(V)	205	205.5	206	mm	
	Depth(D)	--	5.0	5.3	mm	
Weight		--	400	415	g	(2)
Weight			410	425	g	(3)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

(2) Weight without inverter

(3) Weight with inverter.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	200	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

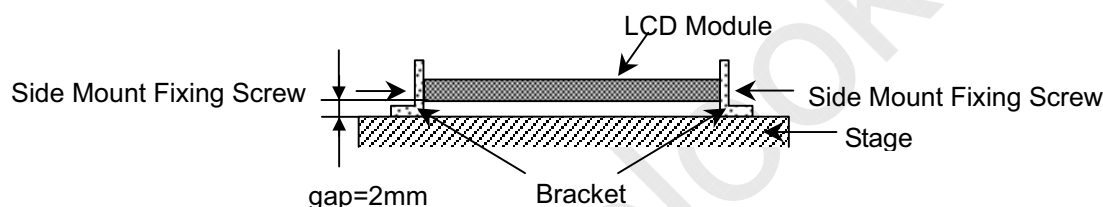
(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

(c) No condensation.

Note (2) The ambient temperature means the temperature of panel surface.

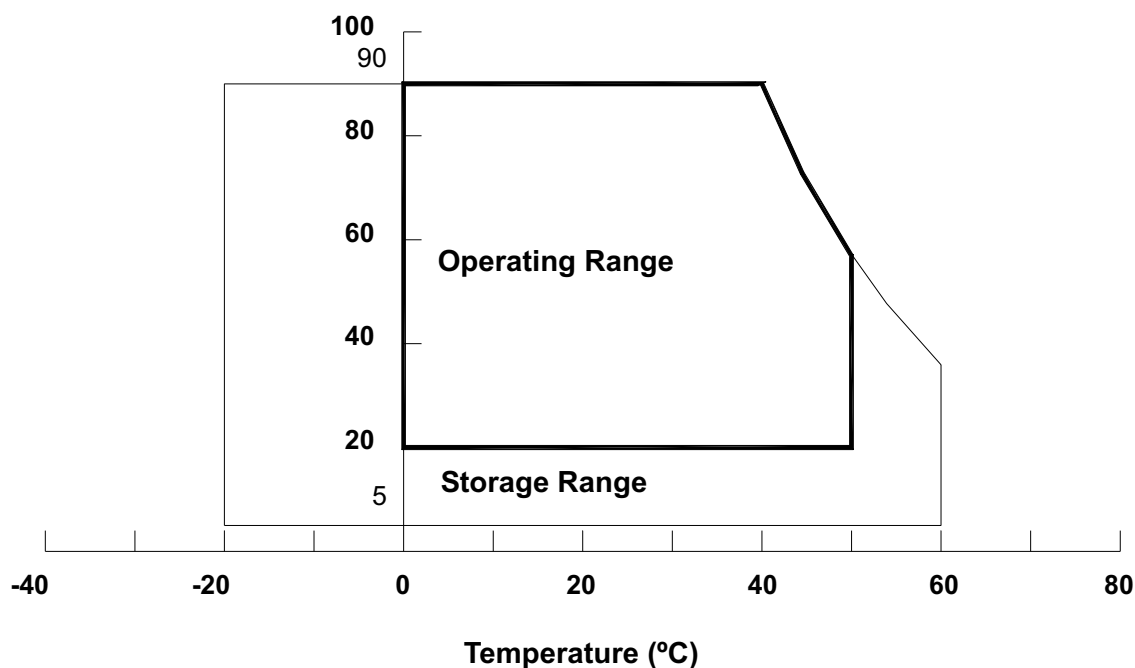
Note (3) 2ms, half sine wave, 1 times for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 500 Hz, Sweep rate 10min, 30min for X, Y, Z. The fixing condition is shown as below:



Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough

Relative Humidity (%RH)



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	$V_{CC}+0.3$	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), $I_L = 6.0 \text{ mA}$
Lamp Current	I_L	-	6.5	mA_{RMS}	
Lamp Frequency	F_L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

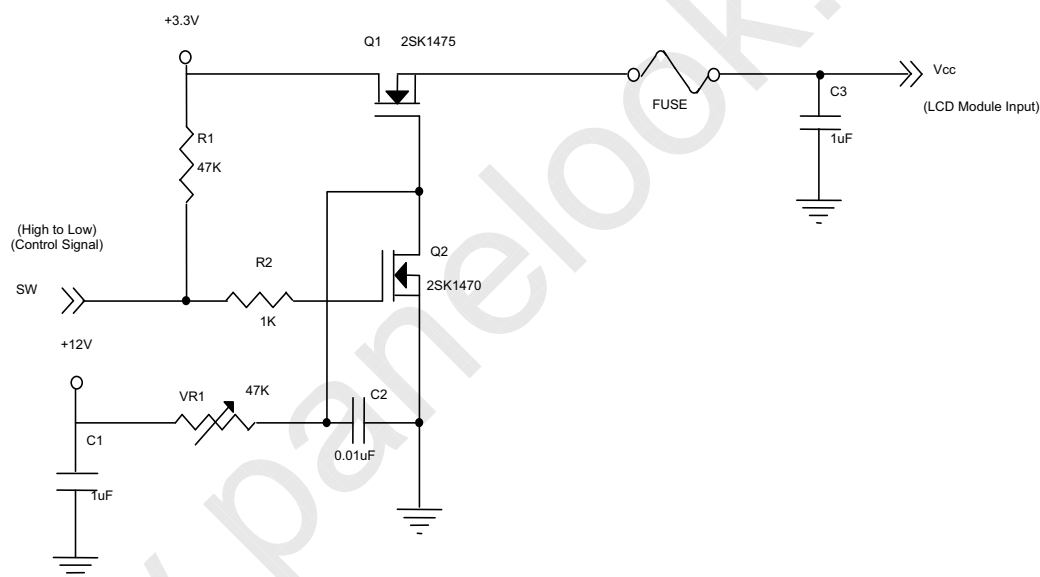
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

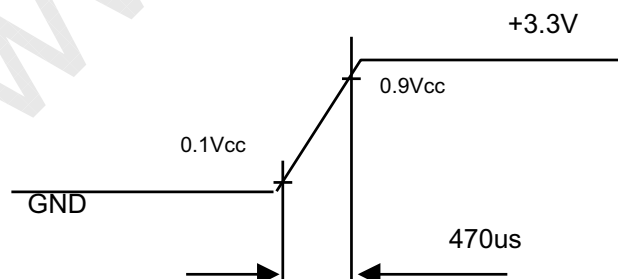
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	3.0	3.3	3.6	V	-
Ripple Voltage		V _{RP}	-	-	100	mV	-
Rush Current		I _{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	I _{CC}	-	335	375	mA	(3)a
	Black		-	400	450	mA	(3)b
Logical Input Voltage	“H” Level	V _{IL}	-	-	+100	mV	-
	“L” Level	V _{IH}	-100	-	-	mV	-
Terminating Resistor		R _T	-	100	-	Ohm	-
Power per EBL WG		P _{EBL}	-	TBD	-	W	(4)

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



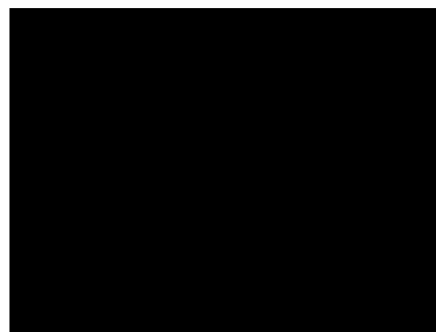
Note (3) The specified power supply current is under the conditions at V_{CC} = 3.3 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

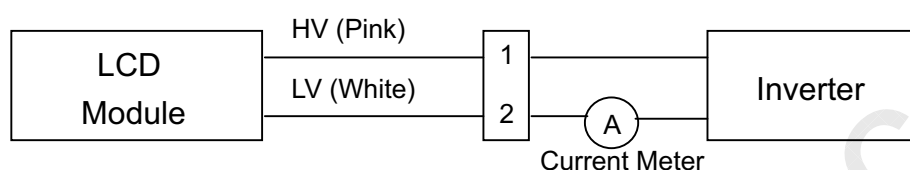
(c) Luminance: 60 nits.

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V _L	603	670	737	V _{RMS}	I _L = 6.0 mA
Lamp Current	I _L	2.0	6.0	6.5	mA _{RMS}	(1)
Lamp Turn On Voltage	V _s	---	---	1360 (25 °C)	V _{RMS}	(2)
		---	---	1500 (0 °C)	V _{RMS}	(2)
Operating Frequency	F _L	50	---	80	KHz	(3)
Lamp Life Time	L _{BL}	15,000	---	---	Hrs	(5)
Power Consumption	P _L	---	4.02	---	W	(4), I _L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ± 2 °C and I_L = 6 mA_{RMS} until one of the following events occurs:

- (a) When the brightness becomes or lower than 50% of its original value.
- (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

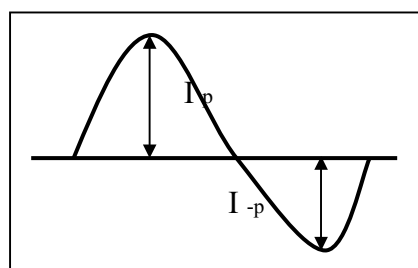
Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter

which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below.
- The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.
- The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

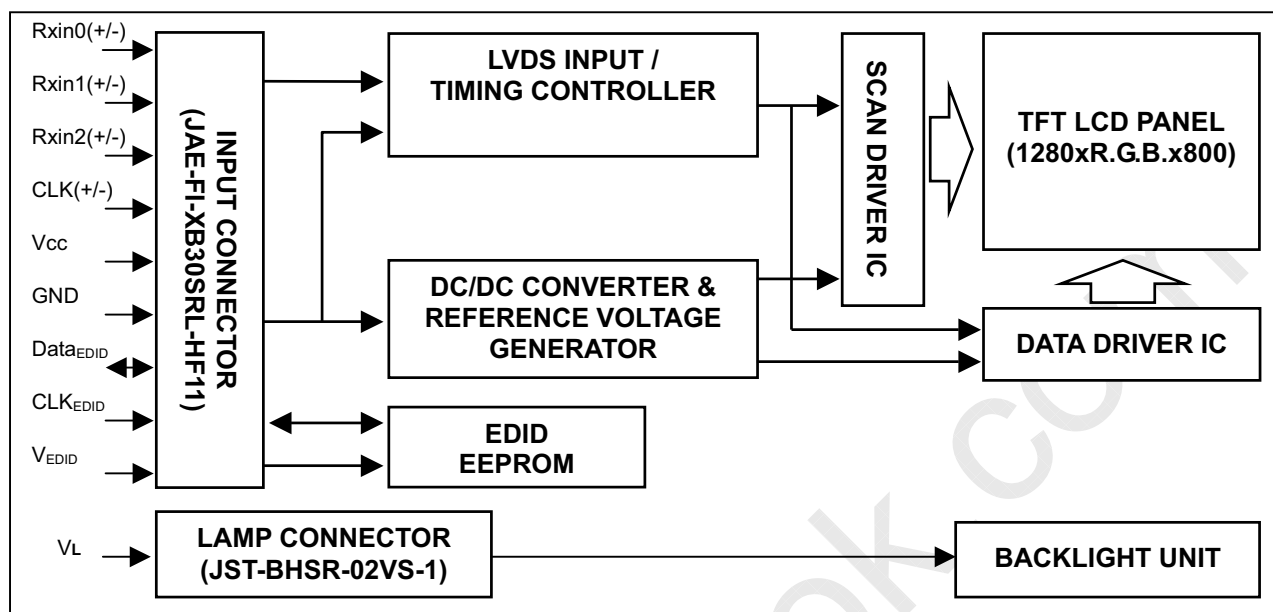
$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	BIST	Panel BIST enable		
6	CLK _{EDID}	DDC Clock		DDC Clock
7	DATA _{EDID}	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5, G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5, DE, Hsync, Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	NC	Non-Connection		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	NC	Non-Connection		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	NC	Non-Connection		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) Connector Part No.: JAE-FI-XB30SL-HF10 or equivalent

Note (2) User's connector Part No: FI-X30C2L or equivalent

Note (3) The first pixel is even.

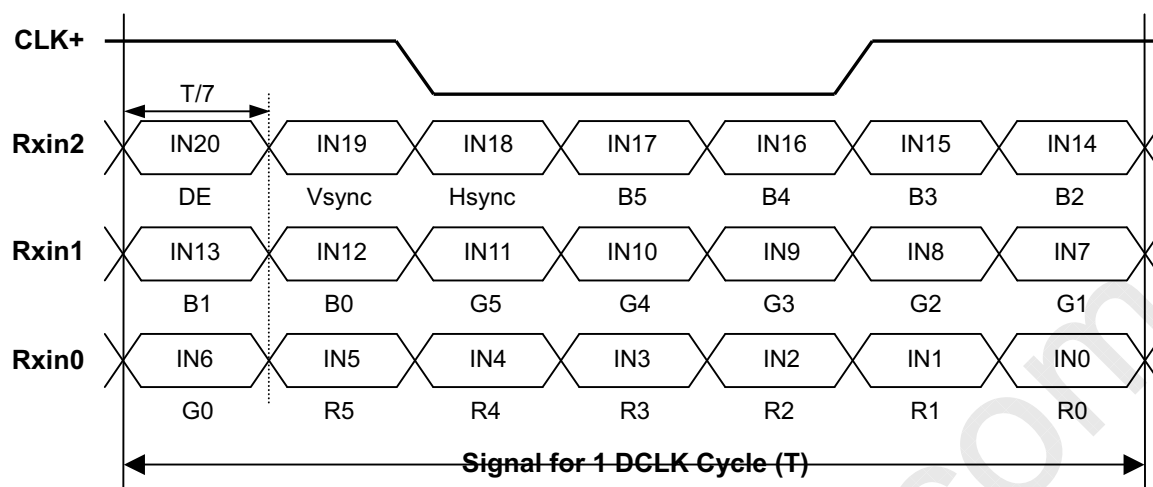
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: JST- BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage



5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

TBD

6. INVERTER SPECIFICATION

6.1 Connector type

Input connector type: **LVC-D20SFYG** (HONDA)

Output connector: **JST SM02B-BHSS-1-TB** (JST)

6.2 Input connector pin assignment

Input Connector pin assignment:

Input connector		Comments
HONDA	LVC-D20SFYG	
Pin	Function	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
5	GND	Ground
6	NC	No Connection
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	INV_PWM	System side PWM input signal for brightness control
13	GND	Ground
14	NC	No Connection
15 ~ 20	NC	No Connection

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.3 Output connector pin assignment

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL
2	CFL-Low	Low-voltage output to the CCFL

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.4 General electrical specification:

6.4.1 Electrical characteristics:

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		4.85	5	5.2	V
3	Input Signal Level for 5VALW	5VALW		4.85	5	5.2	V
4	Input Power	Pin(Max)	Vin=7.5V~21V SMB_DAT=FFH	TBD	TBD	TBD	W
5	Lamp Power	Po	Vin=7.5V~21V SMB_DAT=FFH	TBD	4.02	4.6	W
6	Backlight ON/OFF Control	FPBACK=O N	Enable the inverter	2.0	-	5.25	V
		FPBACK=O FF	Disable the inverter	-0.3	-	0.8	V
7	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus(256 steps dimming control)	00H	-	FFH	-
8	Output Voltage	Vout	IL = 6.0mA(typ)	(603)	(670)	(737)	Vrms
9	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=00H Ta=25℃, after running 30 min.	2.0	2.3	2.6	mA _{rms}
		Iout (Max)	Vin=7.5V~21V SMB_DAT=FFH Ta=25℃, after running 30 min.	5.7	6.0	6.3	mA _{rms}
10	Operation Frequency	Freq	Vin=7.5V~21V	(45)	-	(65)	KHz

11	Burst mode frequency	f_B	Vin=7.5V~21V	200	-	220	Hz
12	Open Lamp Voltage	Vopen	No Load	(1500)	TBD	(1800)	Vrms
13	Striking Time	Ts	No Loadw	0.6	1	1.4	Sec
14	Efficiency	η	Vin=7.5V, SMB_DAT=FFH (RES LOAD=100K ohm)	(80)	-	-	%
15	Start and Delay Time		Vin=14.4V, SMB_DAT=00H	-	130	200	uS
16	Start –up time (Turn on delay time)		Vin=14.4V, SMB_DAT=FFH	-	-	0.1	Sec

- Input Voltage

The operating input voltage of inverter shall be defined.

The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

Enable: At “**ON**” condition (FPBACK=Hi), enable the inverter.

Disable: At “**OFF**” condition (FPBACK=Lo), disable the inverter.

- Quiescent current

At the inverter “**OFF**” condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

The inverter start-up output voltage will be above “**Vopen**” for “**Ts**” minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in “**Ts**” maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Luminance (nits)	10	17	24	30	60	110	150	Max

- Output ripple ratio

$$\text{Ripple ratio} = 2 * (I_{\text{peak}} - I_{\text{valley}}) / (I_{\text{peak}} + I_{\text{valley}}) * 100\%$$

The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(max.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		

$$dI = I_{\text{max}} - I_{\text{min}} \quad \text{or} \quad dI = (I_{\text{max}} - I_{\text{min}}) / I_{\text{Io}}$$

- Output connections short protection

The inverter shall be capable of withstanding the output connections short without damage or over-stress.

And the inverter maximum input power shall be limited within 1W.

6.4.2 Mechanical Drawing

Please refer to CMO's previous mechanical drawing of appendix (07N2737_mech.pdf)

6.4.3 Other Information

- Safety

- The inverter shall meet the requirement of "Limited current circuits" in paragraphs 2.4.1 in IEC60950. There is no fire/smoke while simulating the component of the inverter open/short test.

- The Inverter AND panel must be UL certified with CB certificate and LCC (Limited Current Circuit) test and test reports from UL. Inverter panel combo must pass Dell Safety requirements.

- EMI

The inverter must meet the radiated limitation requirement of CISPR22 class B, FCC-B and VCCI level II with 6dB margin minimum while the inverter operating in the complete system.

- Environment Regulation

- Follow the RoHS requirement.

- Fill in CMO's official document <<Environmentally Conscious Products Questionnaire for Suppliers of Materials, Parts, and Products>> and turn in to CMO before CMO's specification approval process.

- Dell's other requirements

- The inverter must not emit any audible noise.

- Please refer to CMO's official document. "General Inverter Specification for LCD Module" for other general information such as reliability test, safety and etc..



3. Please also refer to DELL's official document about inverter:

- DELL's Generic Inverter Specification, Rev. X00-00 -4.
- DELL's LCD Inverter Qualification Plan, Rev. X04.

Confidential Notice

Remind that all the information described in this document is confidential. Please don't reveal to other people else before getting CMO's agreement.

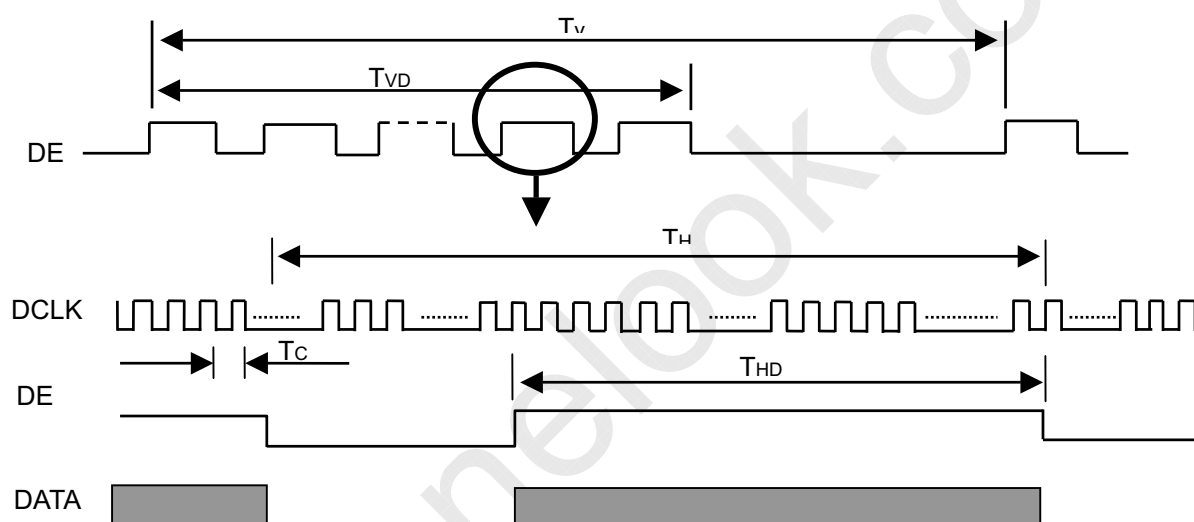
7. INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

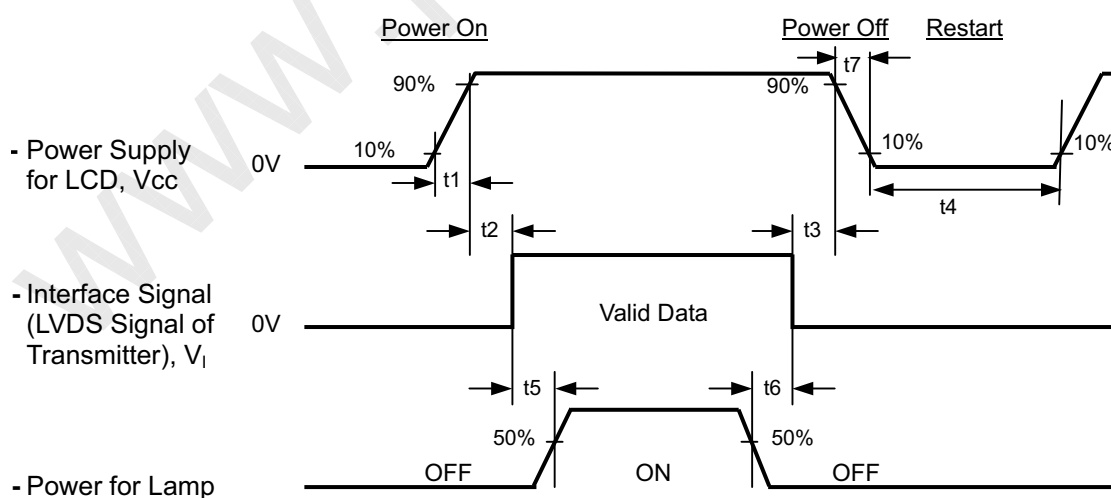
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	71.1	80	MHz	-
DE	Vertical Total Time	TV	810	823	2000	TH	-
	Vertical Addressing Time	TVD	800	800	800	TH	-
	Horizontal Total Time	TH	1360	1440	1900	Tc	-
	Horizontal Addressing Time	THD	1280	1280	1280	Tc	-

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$0.5 < t_1 \leq 10 \text{ msec}$$

$$0 < t_2 \leq 50 \text{ msec}$$

$$0 < t_3 \leq 50 \text{ msec}$$

$$t_4 \geq 500 \text{ msec}$$

$$t_5 \geq 200 \text{ msec}$$

$$t_6 \geq 200 \text{ msec}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

$$t_7 \geq 5 \text{ msec}$$

8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

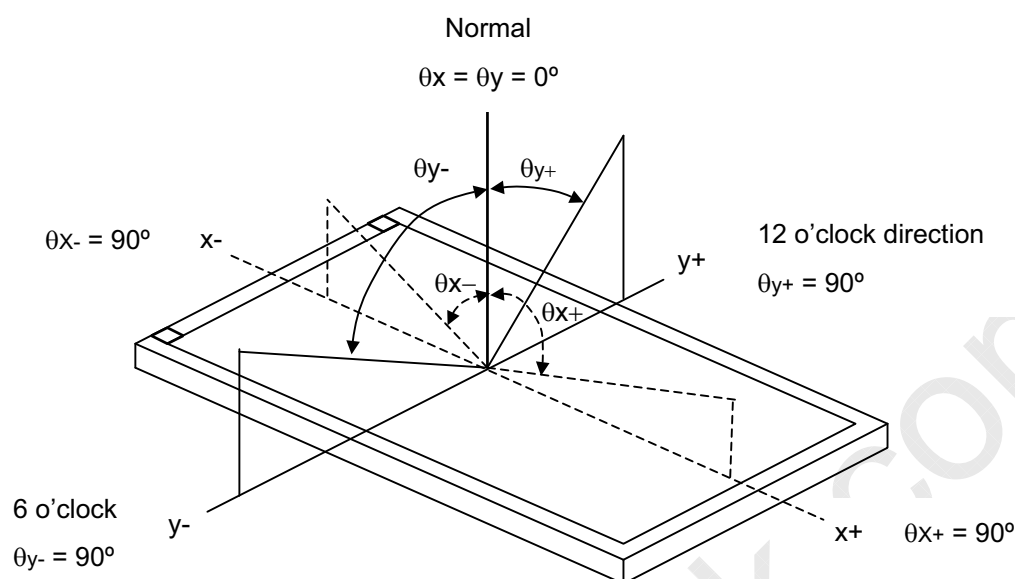
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	6	mA
Inverter Driving Frequency	F _L	61	KHz
Inverter	H05-4915		

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	300	400		-	(2), (5)
Response Time		T _R		-	5	10	ms	(3)
		T _F		-	11	16	ms	
Average Luminance of White		L _{AVE}		150	185		cd/m ²	(4), (5)
White Variation		ΔW				1.4	-	(5), (6)
Color Chromaticity	Red	R _x		TYP -0.03	0.588	TYP +0.03	-	(1)
		R _y			0.337		-	
	Green	G _x			0.315		-	
		G _y			0.534		-	
	Blue	B _x			0.152		-	
		B _y			0.130		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
Viewing Angle	Horizontal	θ _{x+}	CR≥10	40	45		Deg.	
		θ _{x-}		40	45			
	Vertical	θ _{y+}		15	20			
		θ _{y-}		40	45			

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

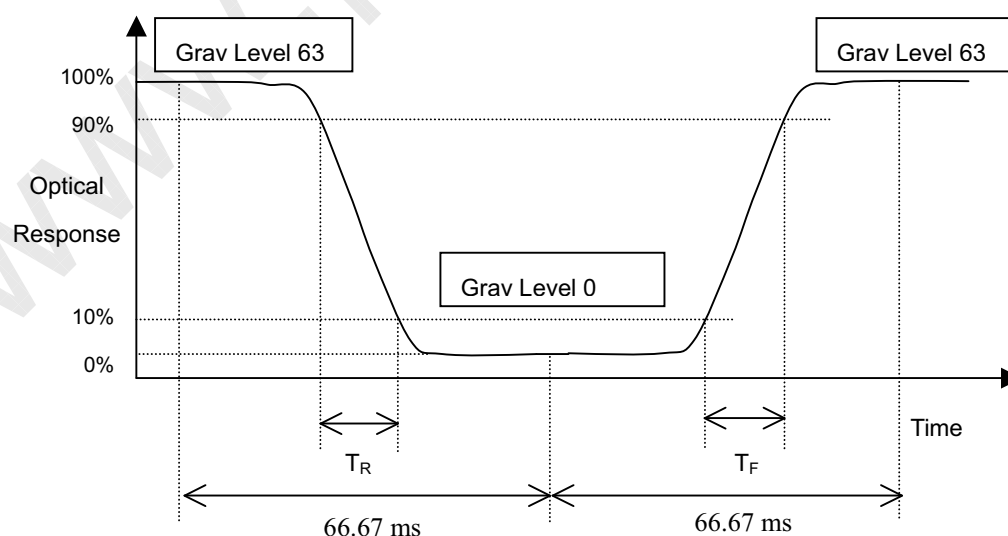
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$CR = CR(5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

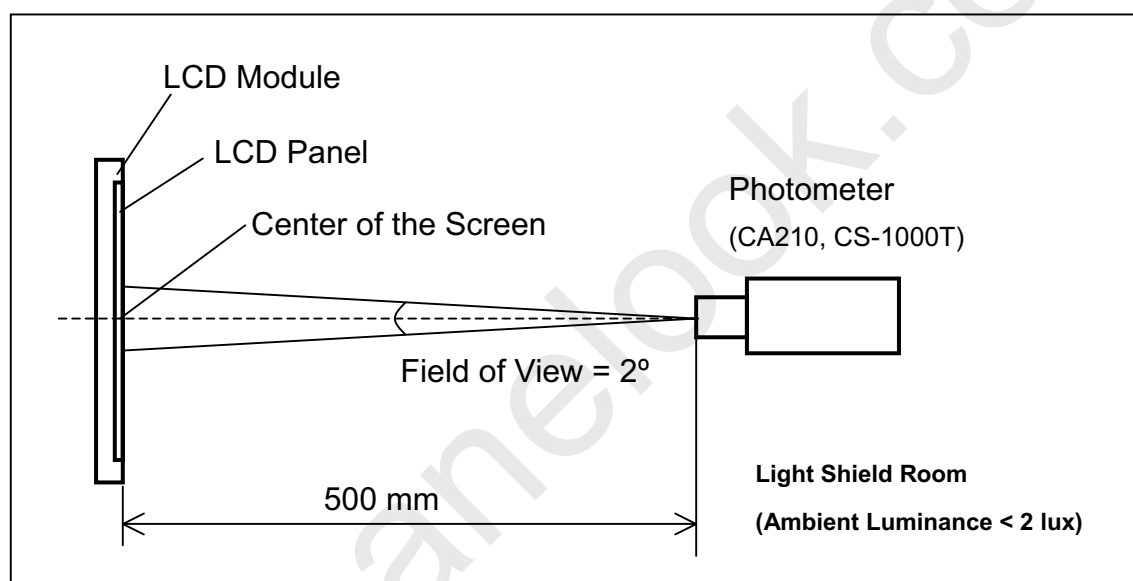
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

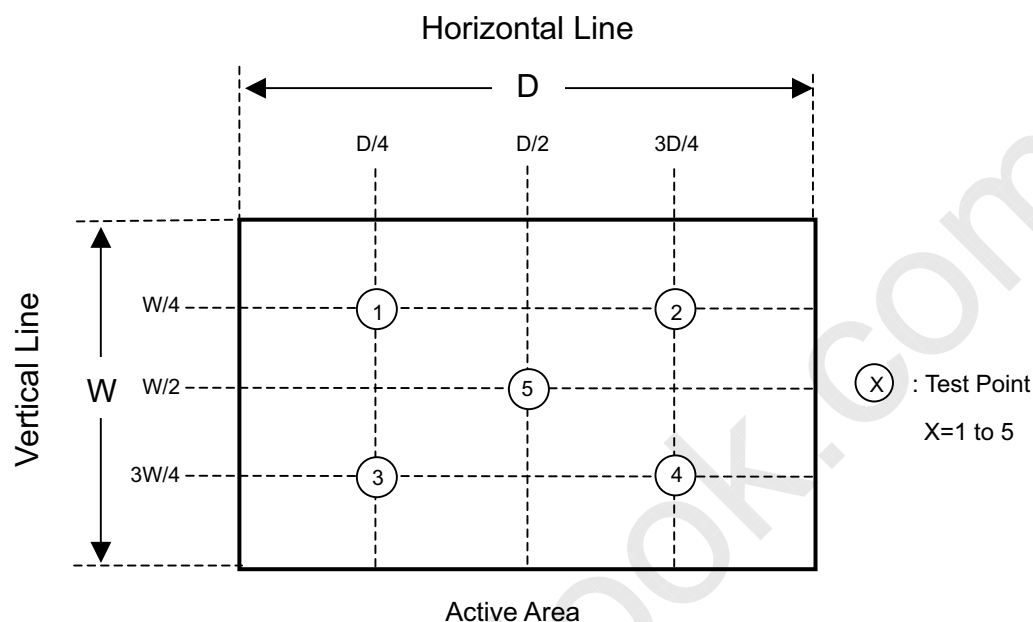
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W = \text{Maximum } [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum } [L(1), L(2), L(3), L(4), L(5)]$$



9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

9.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

10. PACKAGING

9.1 CARTON

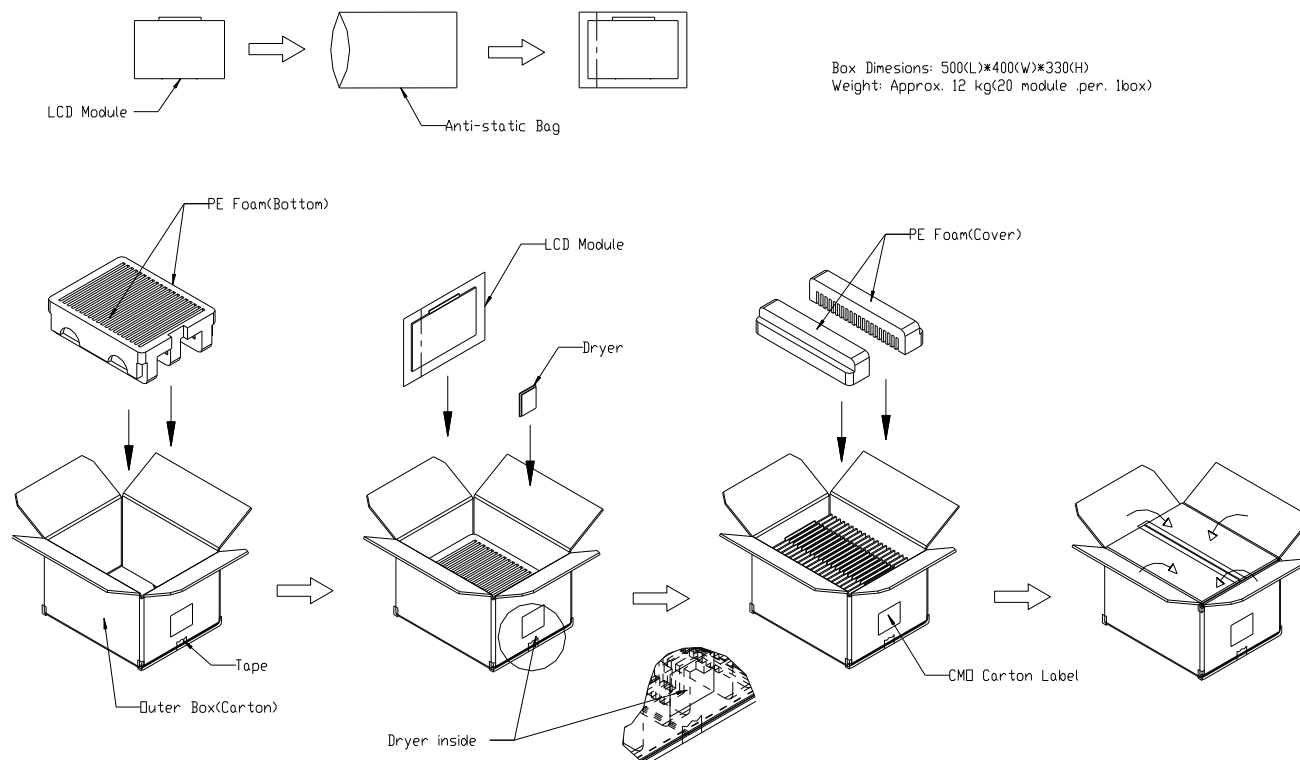


Figure. 9-1 Packing method

9.2 PALLET

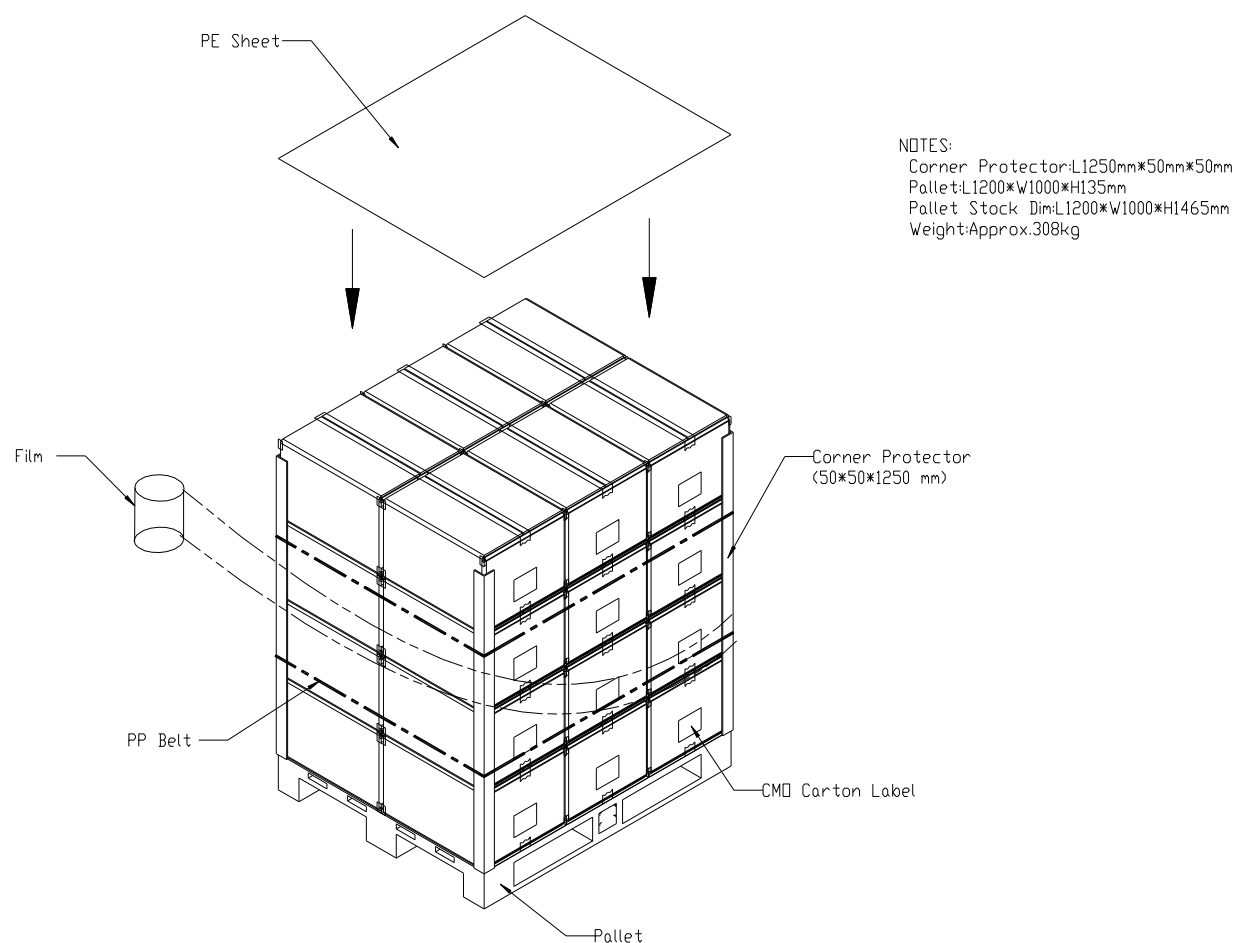


Figure. 9-2 Packing method

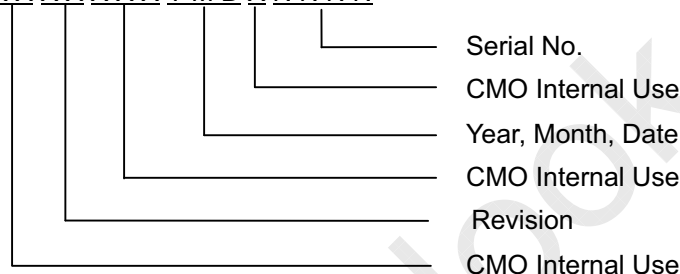
11. DEFINITION OF LABELS

11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



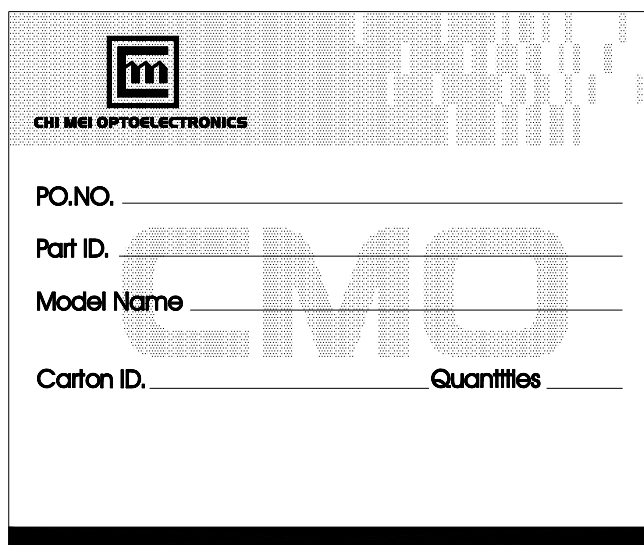
- (a) Model Name: N141I1 - L04
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

11.2 CMO CARTON LABEL



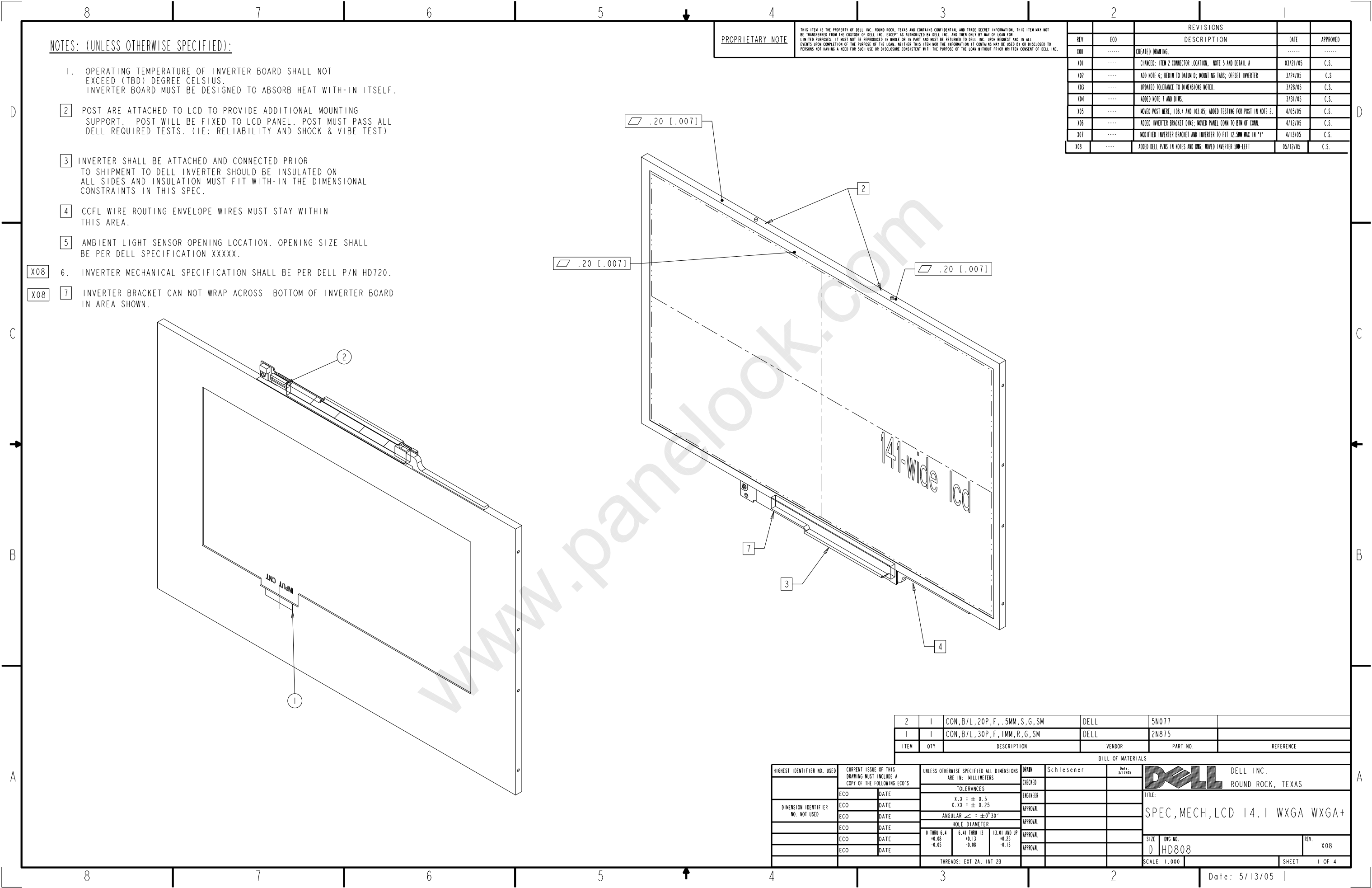
CHI MEI OPTOELECTRONICS

PO.NO. _____

Part ID. _____

Model Name _____

Carton ID. _____ Quantities _____



NOTES: (UNLESS OTHERWISE SPECIFIED):

1. OPERATING TEMPERATURE OF INVERTER BOARD SHALL NOT EXCEED (TBD) DEGREE CELSIUS. INVERTER BOARD MUST BE DESIGNED TO ABSORB HEAT WITH-IN ITSELF.
2. POST ARE ATTACHED TO LCD TO PROVIDE ADDITIONAL MOUNTING SUPPORT. POST WILL BE FIXED TO LCD PANEL. POST MUST PASS ALL DELL REQUIRED TESTS. (IE: RELIABILITY AND SHOCK & VIBE TEST)
3. INVERTER SHALL BE ATTACHED AND CONNECTED PRIOR TO SHIPMENT TO DELL INVERTER SHOULD BE INSULATED ON ALL SIDES AND INSULATION MUST FIT WITH-IN THE DIMENSIONAL CONSTRAINTS IN THIS SPEC.
4. CCFL WIRE ROUTING ENVELOPE WIRES MUST STAY WITHIN THIS AREA.
5. AMBIENT LIGHT SENSOR OPENING LOCATION. OPENING SIZE SHALL BE PER DELL SPECIFICATION XXXXX.
- X08 6. INVERTER MECHANICAL SPECIFICATION SHALL BE PER DELL P/N HD720.
- X08 7. INVERTER BRACKET CAN NOT WRAP ACROSS BOTTOM OF INVERTER BOARD IN AREA SHOWN.

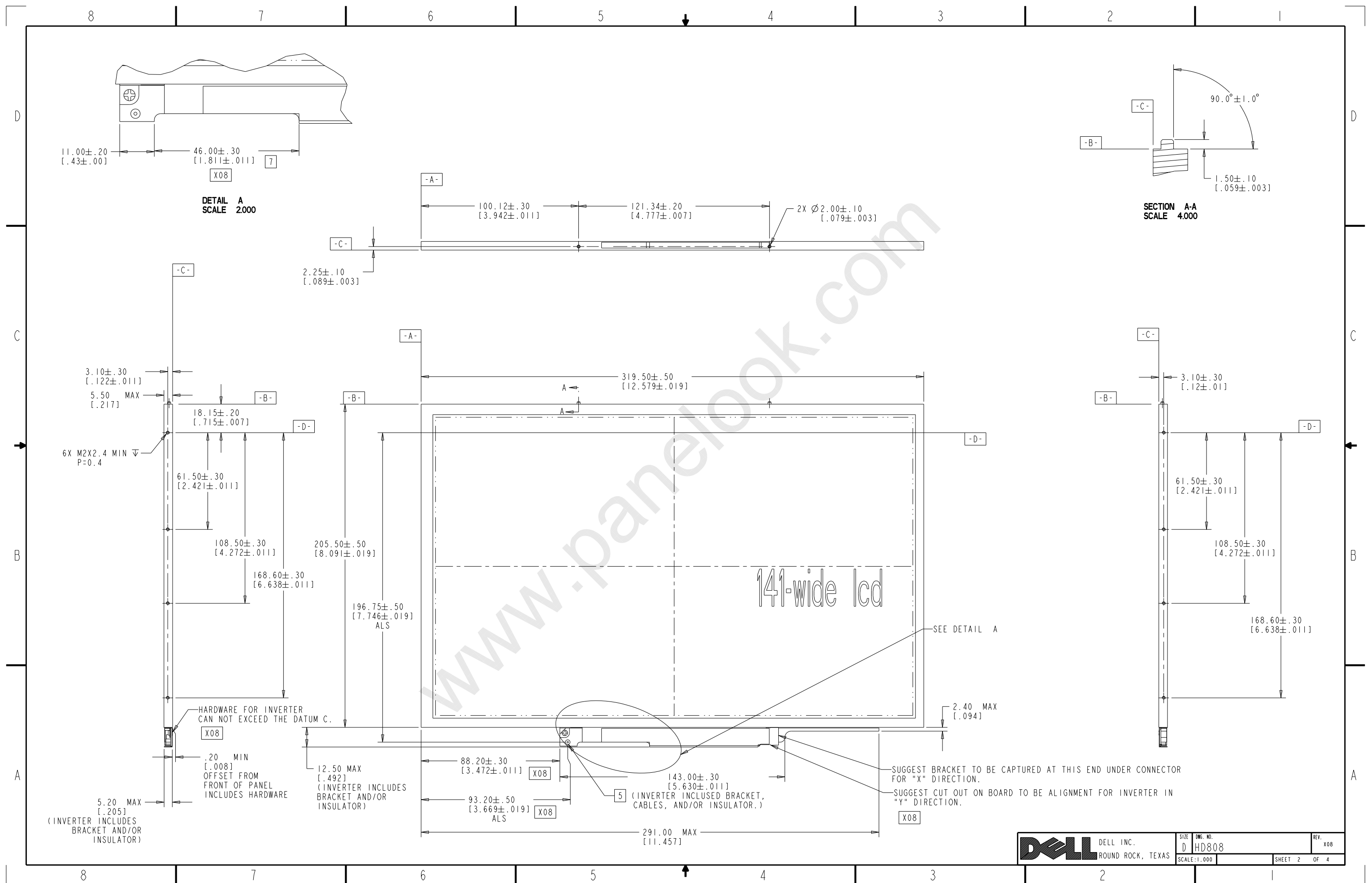
PROPRIETARY NOTE

THIS ITEM IS THE PROPERTY OF DELL INC. ROUND ROCK, TEXAS AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS ITEM MAY NOT BE TRANSFERRED FROM THE CUSTODY OF DELL INC. EXCEPT AS AUTHORIZED BY DELL INC. AND THEN ONLY BY WAY OF LOAN FOR LIMITED PURPOSES. IT MUST NOT BE REPRODUCED IN WHOLE OR IN PART AND MUST BE RETURNED TO DELL INC. UPON REQUEST AND IN ALL EVENTS UPON COMPLETION OF THE PURPOSE OF THE LOAN. NEITHER THIS ITEM NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO PERSONS NOT HAVING A NEED FOR SUCH USE OR DISCLOSURE CONSISTENT WITH THE PURPOSE OF THE LOAN WITHOUT PRIOR WRITTEN CONSENT OF DELL INC.

REVISIONS				
REV	ECO	DESCRIPTION	DATE	APPROVED
X00	-----	CREATED DRAWING.	-----	-----
X01	----	CHANGED: ITEM 2 CONNECTOR LOCATION, NOTE 5 AND DETAIL A	03/21/05	C.S.
X02	----	ADD NOTE 6; REDIN TO DATUM D; MOUNTING TABS; OFFSET INVERTER	3/24/05	C.S.
X03	----	UPDATED TOLERANCE TO DIMENSIONS NOTED.	3/28/05	C.S.
X04	----	ADDED NOTE 7 AND DIMS.	3/31/05	C.S.
X05	----	MOVED POST WERE, 108.4 AND 103.85; ADDED TESTING FOR POST IN NOTE 2.	4/05/05	C.S.
X06	----	ADDED INVERTER BRACKET DIMS; MOVED PANEL CONN TO BTM OF CONN.	4/12/05	C.S.
X07	----	MODIFIED INVERTER BRACKET AND INVERTER TO FIT 12.5MM MAX IN "Y"	4/13/05	C.S.
X08	----	ADDED DELL PINS IN NOTES AND DIMS; MOVED INVERTER 5MM LEFT	05/12/05	C.S.

2	1	CON,B/L,20P,F,.5MM,S,G,SM	DELL	5N077	
1	1	CON,B/L,30P,F,1MM,R,G,SM	DELL	2N875	
ITEM	QTY	DESCRIPTION	VENDOR	PART NO.	REFERENCE
BILL OF MATERIALS					
HIGHEST IDENTIFIER NO. USED	CURRENT ISSUE OF THIS DRAWING MUST INCLUDE A COPY OF THE FOLLOWING ECO'S		UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN: MILLIMETERS		DATE: 3/17/05
DIMENSION IDENTIFIER NO. NOT USED	ECO	DATE	TOLERANCES	CHECKED	DATE
	ECO	DATE	X.X ± 0.5	ENGINEER	
	ECO	DATE	X.XX ± 0.25	APPROVAL	
	ECO	DATE	ANGULAR ± 0° 30'	APPROVAL	
	ECO	DATE	HOLE DIAMETER	APPROVAL	
	ECO	DATE	0 THRU 6.4 +0.08 -0.05	APPROVAL	
	ECO	DATE	6.41 THRU 13 +0.13 -0.08	APPROVAL	
	ECO	DATE	13.01 AND UP +0.25 -0.13	APPROVAL	
			THREADS: EXT 2A, INT 2B		
				SIZE	REV. X08
				DWG NO. D HD808	
				SCALE 1:000	SHEET 1 OF 4

Date: 5/13/05

**DELL**DELL INC.
ROUND ROCK, TEXASSIZE: D
DWG. NO.: HD808
SCALE: 1:1.000

REV. X08

SHEET 2 OF 4

